PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
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PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

	Date of mailing (*day/month/year*) 22 JUL 2009
Applicant's or agent's file reference 5087-1083	FOR FURTHER ACTION See paragraph 2 below

International application No.	International filing date (*day/month/year*)	Priority date (*day/month/year*)
PCT/US08/60695	17 April 2008 (17.04.2008)	17 April 2007 (17.04.2007)

International Patent Classification (IPC) or both national classification and IPC

IPC: **H03K 19/173**(2006.01)
USPC: 326/38

Applicant

CYPRESS SEMICONDUCTOR CORPORATION

1. This opinion contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☒	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(*b*) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/ US	Date of completion of this opinion	Authorized officer
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (571) 273-3201	18 July 2009 (18.07.2009)	Clay Laballe Telephone No. (571) 272-1594

Form PCT/ISA/237 (cover sheet) (April 2007)

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Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

☒ the international application in the language in which it was filed

☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

a. type of material

☐ a sequence listing

☐ table(s) related to the sequence listing

b. format of material

☐ on paper

☐ in electronic form

c. time of filing/furnishing

☐ contained in the international application as filed.

☐ filed together with the international application in electronic form.

☐ furnished subsequently to this Authority for the purposes of search.

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

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Box No. IV Lack of unity of invention

1. ☒ In response to the invitation (Form PCT/ISA/206) to pay additional fees the applicant has, within the applicable time limit:
   - ☐ paid additional fees
   - ☐ paid additional fees under protest and, where applicable, the protest fee
   - ☐ paid additional fees under protest but the applicable protest fee was not paid
   - ☒ not paid additional fees
2. ☐ This Authority found that the requirement of unity of invention is not complied with and chose not to invite the applicant to pay additional fees.
3. This Authority considers that the requirement of unity of invention in accordance with Rule 13.1, 13.2 and 13.3 is
   - ☐ complied with
   - ☒ not complied with for the following reasons:

   See the lack of unity section of the International Search Report(Form PCT/ISA/210)

4. Consequently, this opinion has been established in respect of the following parts of the international application:
   - ☐ all parts.
   - ☒ the parts relating to claims Nos. 1-18

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Box No. V Reasoned statement under Rule 43 *bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims 4-5, 7, 10-13, 17	YES
	Claims 1-3, 6, 8-9, 14-16, 18	NO
Inventive step (IS)	Claims 4-5, 7, 10-13, 17	YES
	Claims 1-3, 6, 8-9, 14-16, 18	NO
Industrial applicability (IA)	Claims 1-18	YES
	Claims NONE	NO

2. Citations and explanations:

Please See Continuation Sheet

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Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

V. 2. Citations and Explanations:

Claims 1-3, 6, 8-9, and 14-16 lack novelty under PCT Article 33(2) as being anticipated by Azegami et al. (6,404,224).

Claim 1, Azegami shows an apparatus (Figs. 46 or 59), comprising:

different functional dements (223 and 50, Fig. 46) all located in a same integrated circuit wherein at least one of the functional elements comprises a microcontroller (223);

configuration registers or configuration memory (222 and 225) in the integrated circuit to store configuration values loaded by the micro-controller;

connectors configured to connect the integrated circuit to external signals (input/output not shown in the figures, but showing figure 32B); and

a system level interconnect (90, 221) located in the integrated circuit to programmably connect together the different functional elements and different connectors according to the configuration values loaded into the configuration registers or configuration memory by the micro-controller (col. 26, lines 44-50 and 60-65).

Claim 2, Azegami shows the apparatus according to claim 1 wherein the system level interconnect dynamically changes the connections between the different functional elements and the different connectors in real time (may be changed at any time, col. 60- 65) according to different operational states of the integrated circuit.

Claim 3, Azegami shows the apparatus according to claim 1 wherein the system level interconnect is configured to connect any of the different functional elements in the integrated circuit to any of the different connectors and further configured to connect any of the different functional elements to any of the other functional elements according to the configuration values (86-1, Fig. 32B for connectors and 95, Fig. 34B for interconnect).

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Supplemental Box
In case the space in any of the preceding boxes is not sufficient.

Claim 6, Azegami shows the apparatus according to claim 1 wherein: the system level interconnect is configured to operate a selected one of the connectors as an input pin (82, Fig. 32B) by coupling the selected connector to an input for one of the functional elements while the integrated circuit is in a first operational state (I/O pin connected to any one of the logic cell through horizontal and vertical by programmable switches shown as circles in figure 32B as input); and

the system level interconnect is further configured to operate the same selected connector as an output pin (82, Fig. 32B) by coupling the same selected connector to an output for one of the functional elements while the integrated circuit is in a second operational state (I/O pin connected to any one of the logic cell through horizontal and vertical by programmable switches shown as circles in figure 32B as output).

Claim 8, Azegami shows the apparatus according to claim 1 wherein the system level interconnect compnses horizontal channels (vertical lines) configured to programmably couple to the different functional elements according to the configuration values in the configuration registers or configuration memory (225, Fig. 46); and

programmable couple to the different connectors (not shown in the figure 46, but shown in figure 32B) according to the configuration values in the configuration registers or configuration memory (86-1 and 86-2).

Claim 9, Azegami shows the apparatus according to claim 8 further comprising: channel switches (not shown in the figure, but inherent elements that are connected to the logic cells inputs and output by vertical lines, for example, see Fig. 32B that have a plurality of switches as a little circle that can configurable connect to the vertical lines) that programmably couple the horizontal channels to the different functional elements according to the configuration values; and

segmentation switches (little squares on the vertical lines, Fig. 34A) that programmably couple the horizontal channels to each other according to the configuration values.

Claims 14-15, refer to claims 1-3 and 8 above.

Claim 16, Azegami shows the integrated circuit according to claim 15 further comprising segmentation elements (little squares on the vertical lines, Fig. 34A) that programmably couple together the channels according to the configuration values.

Claim 18 lacks an inventive step under PCT Article 33(3) as being obvious over Azegami et al. (6,404,224) in view of Wojke (2003/0055852).

Azegami discloses the claimed invention except for a logic block the each includes uncommitted programmable logic sections and structural arithmetic logic sections.

Wojke discloses a logic block includes uncommitted programmable logic sections (32 or four look up tables, Fig. 3) and structural arithmetic logic sections (68 and 70).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide the logic cell of Azegami with four look up tables and the arithmetic logic sections of Wojke, in order to perform highly mathematical intensive operation and effectively.

Claims 4-5, 7, 10-13, and 17 meet the criteria set out in PCT Article 33(2)-(3), because the prior art does not teach or fairly suggest different functional elements that are all located on a same integrated circuit wherein at least one of the functional elements comprises a micro-controller. Configuration registers or configuration memory in the integrated circuit store configuration values loaded by the micro-controller. Connectors are configured to connect the integrated circuit to external signals. A system level interconnect also located in the integrated circuit programmably connects together the different functional elements and different connectors according to the configuration values loaded into the configuration registers.

Claims 1-18 meet the criteria set out in PCT 33(4), and thus have industrial applicability because the claimed subject matter can be made or used in industry.